AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) An interface between memory and an integrated circuit, comprising:

   a write path comprising a write data path and a forwarded clock path, wherein data propagated through the write path is synchronized by a clock signal; [[and]]

   a read path comprising a read data path [[,]] ;

   ~~wherein data propagated through the write path and read path is synchronized by a clock signal~~

   circuitry configured to measure accumulated phase of data on the read data path relative to the clock signal and further configured to compensate for the accumulated phase, wherein data propagated through the read path is synchronized by the clock signal based on the circuitry.

2. (Currently Amended) The interface of claim 1, wherein the write data path synchronizes operations with the forwarded clock path, and wherein the forwarded clock path uses ~~and read data path use~~ the clock signal as a time reference.

3. (Original) The interface of claim 1, wherein the clock signal is provided by the integrated circuit.

4. (Original) The interface of claim 1, wherein the read path and write path operatively connect the memory and the integrated circuit.

5. (Original) The interface of claim 1, wherein the memory is SDRAM.

6. (Original) The interface of claim 1, wherein the integrated circuit comprises a texture engine.

7. (Original) The interface of claim 1, wherein the write data path comprises circuitry having a first data propagation time, wherein the forwarded clock path comprises circuitry having a second data propagation time, and wherein the first data propagation time is substantially equal to the second data propagation time.

8. (Currently Amended) The interface of claim 1, wherein the ~~read data path comprises:~~ circuitry is pipeline circuitry adapted to compensate for accumulated phase generated by data propagation through the read data path.

9. (Original) The interface of claim 8, wherein the pipeline circuitry inputs at least one clock signal, and wherein the at least one clock signal is dependent on the clock signal.

10. (Currently Amended) A computer system having an interface dependent on a clock signal and having a write path and a read path comprising:

a memory;[[,]] and

an integrated circuit,

wherein the interface operatively connects the memory and integrated circuit, synchronizes write data propagating through the write path with a first clock signal propagating through the write data path, and synchronizes read data propagating through the read path with a second clock signal by measuring accumulated phase of the read data relative to the second clock signal and compensating for the accumulated phase.

11. (Original) The computer system of claim 10, wherein the first clock signal is derived from the second clock signal.

12. (Currently Amended) A method for synchronizing data propagation through an interface connecting memory and an integrated circuit, the interface having a write path and a read path, comprising:

propagating data through a write data path, wherein the write path comprises the write data path and a forwarded clock path;

propagating a clock signal through the forwarded clock path;

synchronizing the data propagation through the write data path to the forwarded clock path;

propagating read data through a read data path, wherein the read path comprises the read data path; and

synchronizing the read data propagation through the read data path to the clock signal by measuring accumulated phase of the read data relative to the clock signal and compensating for the accumulated phase.

13. (Original) The method of claim 12, wherein the clock signal is received from the integrated circuit.

14. (Original) The method of claim 12, wherein the memory is SDRAM.

15. (Original) The method of claim 12, wherein the integrated circuit comprises a texture engine.

16. (Original) The method of claim 12, wherein the read path and write path operatively connect the memory and the integrated circuit.

17. (Original) The method of claim 12, wherein a first amount of delay is needed to propagate a first amount of data through the write data path, wherein a second amount of delay is needed to propagate a second amount of data through the forwarded clock path, and wherein the first amount of delay is substantially equal to the second amount of delay.

18. (Cancelled)